What is claimed is:

[Claim 1] A field effect transistor comprising:

a silicon substrate, wherein the top surface of said silicon substrate has an increased oxygen content when compared to other portions of said silicon substrate, and wherein said oxygen content of said top surface of said silicon substrate is below an amount that would prevent epitaxial growth;
an epitaxial silicon layer above said top surface of said silicon substrate; and
a gate stack above said epitaxial silicon layer.

[Claim 2] The field effect transistor in claim 1, wherein source/drain and halo dopants are substantially limited to said epitaxial silicon layer.

[Claim 3] The field effect transistor in claim 1, wherein said increased oxygen content limits dopants within said epitaxial silicon layer from moving into said silicon substrate.

[Claim 4] The field effect transistor in claim 1, wherein said epitaxial silicon layer comprises an in-situ doped epitaxial silicon layer.

[Claim 5] The field effect transistor in claim 1, further comprising source/drain regions in said epitaxial silicon layer.

[Claim 6] The field effect transistor in claim 1, further comprising isolation regions in said epitaxial silicon layer and said silicon substrate.

[Claim 7] The field effect transistor in claim 1, further comprising sidewall spacers on said gate conductor.

[Claim 8] A field effect transistor comprising:

a silicon substrate, wherein the top surface of said silicon substrate has an increased oxygen content when compared to other portions of said silicon substrate, and wherein said oxygen content of said top surface of said silicon substrate is below an amount that would prevent epitaxial growth;
an epitaxial silicon halo layer on said top of said silicon substrate;
an epitaxial silicon source/drain layer on said epitaxial silicon halo layer; and
a gate stack above said epitaxial silicon source/drain layer.

[Claim 9] The field effect transistor in claim 8, wherein source/drain dopants are substantially limited to said epitaxial silicon source/drain layer.

[Claim 10] The field effect transistor in claim 8, wherein said increased oxygen content substantially limits dopants within said epitaxial silicon layer from moving into said silicon substrate.

[Claim 11] The field effect transistor in claim 8, wherein said silicon substrate includes a column portion extending through said epitaxial silicon panel layer and said epitaxial silicon source/drain layer, wherein said column portion is below said gate conductor.

[Claim 12] The field effect transistor in claim 8, wherein halo dopants are substantially limited to said epitaxial silicon halo layer.

[Claim 13] The field effect transistor in claim 8, further comprising isolation regions in said epitaxial silicon layer and said silicon substrate.

[Claim 14] The field effect transistor in claim 8, further comprising sidewall spacers on said gate conductor.

[Claim 15] A method of forming a field effect transistor, said method comprising:

increasing the oxygen content of the top surface of a silicon substrate when compared to other portions of the silicon substrate, wherein said oxygen content of said top surface of said silicon substrate is below an amount that would prevent epitaxial growth;
epitaxially growing an epitaxial silicon layer on said top surface of said silicon substrate;
forming a gate stack on said epitaxial silicon layer; and
delivering dopants into regions of said epitaxial silicon layer not protected by said gate stack.

[Claim 16] The method in claim 15, further comprising cleaning said top surface of said silicon substrate before increasing the oxygen content of said top surface of said silicon substrate.

[Claim 17] The method in claim 15, further comprising forming isolation regions in said epitaxial silicon layer and said silicon substrate.

[Claim 18] The method in claim 15, wherein said process of delivering said dopants comprises one of implanting said dopants and diffusing said dopants.

[Claim 19] The method in claim 15, further comprising annealing said transistor to activate said dopants.

[Claim 20] The method in claim 15, wherein said process of forming said gate stack comprises:

patterning a gate stack on said epitaxial silicon layer; and
forming sidewall spacers on said gate conductor.

[Claim 21] The method in claim 15, wherein said process of delivering said dopants avoids delivering said dopants to said silicon substrate.

[Claim 22] A method of forming a field effect transistor, said method comprising:

forming a gate stack on a silicon substrate;
etching the top surface of said silicon substrate not protected by said gate stack to reduce the height of said top surface below the bottom of said gate stack;
increasing the oxygen content of said top surface of said silicon substrate when compared to other portions of the silicon substrate, wherein said oxygen content of said top surface of said silicon substrate is below an amount that would prevent epitaxial growth; and
epitaxially growing an epitaxial silicon layer on said top surface of said silicon substrate.

[Claim 23] The method in claim 22, wherein said process of growing said epitaxial silicon layer comprises growing an in-situ doped epitaxial silicon layer.

[Claim 24] The method in claim 22, wherein said process of growing said epitaxial silicon layer comprises:

epitaxially growing an in-situ doped epitaxial silicon halo layer on said top of said silicon substrate; and
epitaxially growing an in-situ doped epitaxial silicon source/drain layer on said epitaxial silicon halo layer.

[Claim 25] The method in claim 24, wherein said epitaxial silicon halo layer has the opposite doping of said epitaxial silicon source/drain layer.

[Claim 26] The method in claim 24, further comprising annealing said transistor to activate said dopants.

[Claim 27] The method in claim 22, wherein said process of forming said gate stack comprises:

patterning a gate conductor and dielectric stack on said epitaxial silicon layer; and
forming sidewall spacers on said gate conductor.

[Claim 28] The method in claim 22, wherein said process of etching said top surface of said silicon substrate undercuts said silicon substrate below said gate stack such that regions of said gate stack overhang said top surface of said silicon substrate.